Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-21. (Canceled)

22. (Currently Amended) A receiver for estimation and compensation of phase imbalance or gain imbalance, the receiver comprising:

a QPSK modulation circuit based on a complex scrambling code;

a first circuit coupled to the QPSK modulation circuit and structured ~~adapted~~ to estimate the phase imbalance or gain imbalance of I and Q components of an incoming complex signal prior to symbol synchronization, ~~and~~ the first circuit adapted to generate as an output a ratio between a cross correlation of the ~~product of compensated~~ I and Q components and ~~the~~ a mean value of a square of the ~~compensated~~ I component; and

a second circuit ~~that receives~~ configured to receive as inputs the uncompensated I and Q components and the output of the first circuit and ~~outputs~~ to output on output terminals the compensated I and Q components.

23. (Currently Amended) The receiver of claim 22, wherein the first circuit ~~receives as input~~ is structured to receive as inputs the I and Q components of the complex signal after demodulation and compensation.

24. (Currently Amended) The receiver according to claim 22, wherein the first circuit comprises a low pass filter ~~for~~ structured to low pass ~~filtering of~~ filter the product of the compensated I and Q components and low pass ~~filtering of~~ filter the square of the compensated I component.

25. (Currently Amended) The receiver of claim 22, comprising a synchronizer having ~~inputs~~ input terminals coupled to the ~~outputs~~ output terminals of the second circuit, the synchronizer comprising a UMTS synchronizer.

26. (Currently Amended) ~~The receiver of claim 22, wherein the~~ A receiver for estimation and compensation of phase imbalance or gain imbalance, the receiver comprising:

a QPSK modulation circuit based on a complex scrambling code;

a first circuit structured to estimate the phase imbalance or gain imbalance of I and Q components of an incoming complex signal prior to symbol synchronization, the first circuit structured to generate as an output a ratio of the product of compensated I and Q components and the square of the compensated I component, the first circuit ~~comprises~~ including a first multiplier ~~receiving~~ structured to receive the compensated I and Q signals and ~~generating~~ to generate a product thereof, and a second multiplier ~~that generates~~ structured to generate the square of the compensated I component, a divider ~~that divides~~ structured to divide the product of the first multiplier by the product of the second multiplier, the output of the divider integrated at an integration circuit that outputs an integration signal to the second circuit; and

a second circuit configured to receive as inputs the uncompensated I and Q components and the output of the first circuit and to output on output terminals the compensated I and Q components.

27.-32. (Canceled)

33. (New) The receiver of claim 26, wherein the first circuit is structured to receive as inputs the I and Q components of the complex signal after demodulation and compensation.

34. (New) The receiver according to claim 26, wherein the first circuit comprises a low pass filter structured to low pass filter the product of the compensated I and Q components and low pass filter the square of the compensated I component.

35. (New) The receiver of claim 26, comprising a synchronizer having input terminals coupled to the output terminals of the second circuit, the synchronizer comprising a UMTS synchronizer.

36. (New) A circuit, comprising:

a QPSK modulation circuit structured for a complex searching code;

a first circuit having a first multiplier structured to receive I and Q components of an incoming I/Q modulated signal and a second multiplier structured to receive the I component, and a divider structured to divide an output of the first multiplier by an output of the second multiplier, the first circuit structured to generate as an output a ratio between a cross correlation of the I and Q components and a mean value of a square of the I component.

37. (New) The circuit of claim 36, comprising a second circuit structured to receive an integration signal from the divider circuit in the first circuit and to receive uncompensated I and Q components of the incoming I/Q modulated signal, and to output on an output terminal of the circuit compensated I and Q components.

38. (New) The circuit of claim 37, wherein the first circuit is structured to receive as inputs the I and Q components of a complex signal after demodulation and compensation.

39. (New) The circuit of claim 37, wherein the first circuit comprises a low pass filter structured to low pass filter the output of the first multiplier and a low pass filter structured to filter the output of the second multiplier, the output of both low pass filters received as inputs to the divider of the first circuit.

40. (New) The circuit of claim 37, comprising a synchronizer having input terminals coupled to output terminals of the second circuit, the synchronizer comprising a UMTS synchronizer.

41. (New) The circuit of claim 37, comprising a third circuit having a multiplier structured to receive the Q component, and a divider circuit structured to receive an output of the second multiplier of the first circuit and an output of the multiplier of the third circuit, and further structured to generate as an output a ratio between the output of the second multiplier of the first circuit and the output of the multiplier of the third circuit.

42. (New) The circuit of claim 41, wherein the first circuit is structured to receive as inputs the I and Q components of a complex signal after demodulation and compensation.

43. (New) The circuit of claim 41, wherein the first circuit comprises a low pass filter structured to low pass filter the output of the first multiplier and a low pass filter structured to filter the output of the second multiplier, the output of both low pass filters received as inputs to the divider of the first circuit.

44. (New) the circuit of claim 41, comprising a synchronizer having input terminals coupled to output terminals of the second circuit, the synchronizer comprising a UMTS synchronizer.